CLAIMS

[0054] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating a memory cell, said method comprising the steps of:

forming a conductive layer in a trench of an insulating layer;

forming a dielectric layer over said conductive layer and said insulating layer;

forming an opening in said dielectric layer over said conductive layer;

forming a first magnetic layer in said opening;

planarizing an upper surface of said first magnetic layer and said dielectric layer;

forming a nonmagnetic layer over said first magnetic layer and said dielectric layer;

forming a second magnetic layer over said nonmagnetic layer; and

patterning said second magnetic layer, nonmagnetic layer and said dielectric layer to form a memory cell.

2. The method of claim 1 wherein said opening is a trench.

3. The method of claim 1 wherein said opening is surrounded by said dielectric layer.

4. The method of claim 1 wherein said step of forming said first magnetic member is by electroless plating.

5. The method of claim 4 wherein said plating is performed at about 80^0 – 90^0C.

6. The method of claim 1 wherein said step of planarizing is performed by sputtering.

7. The method of claim 1 wherein said step of planarizing is performed by chemical mechanical polishing.

8. The method of claim 1 wherein said dielectric layer is formed to a thickness of about 2-3 nm thicker than the desired final thickness of said first magnetic layer.

9. The method of claim 1 wherein said first magnetic layer is formed of NiFe.

10. The method of claim 1 wherein said first magnetic layer is a sense layer.

11. The method of claim 10 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.

12. The method of claim 1 wherein said second magnetic layer is a pinned layer.

13. The method of claim 12 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.

14. The method of claim 1 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

15. The method of claim 1 wherein said nonmagnetic layer is aluminum oxide.

16. A method of fabricating a memory cell, said method comprising the steps of:

forming a conductive layer in a trench of an insulating layer;

forming a dielectric layer over said conductive layer and said insulating layer;

forming a opening in said dielectric layer over said conductive layer;

forming a sense layer in said opening;

planarizing an upper surface of said sense layer and said dielectric layer;

forming a tunnel barrier layer over said sense layer and said dielectric layer;

forming a pinned layer over said tunnel barrier layer; and

patterning said pinned layer, said tunnel barrier layer and said dielectric layer to form a memory cell.

17. The method of claim 16 wherein said opening is a trench.

18. The method of claim 16 wherein said opening is surrounded by said dielectric layer.

19. The method of claim 16 wherein said step of forming said sense layer is by electroless plating.

20. The method of claim 19 wherein said plating is performed at about 80^0 – 90^0C.

21. The method of claim 16 wherein said step of planarizing is performed by sputtering.

22. The method of claim 16 wherein said step of planarizing is performed by chemical mechanical polishing.

23. The method of claim 16 wherein said dielectric layer is formed to a thickness of about 2-3 nm thicker than the desired final thickness of said sense layer.

24. The method of claim 16 wherein said sense layer is formed of NiFe.

25. The method of claim 16 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.

26. The method of claim 16 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.

27. The method of claim 16 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

28. The method of claim 16 wherein said nonmagnetic layer is aluminum oxide.

29. A method of fabricating a memory cell, said method comprising the steps of:

forming a conductive layer in a trench of an insulating layer;

forming a dielectric layer over said conductive layer and said insulating layer;

forming an opening in said dielectric layer over said conductive layer;

electroplating a sense layer in said opening;

planarizing an upper surface of said sense layer and said dielectric layer;

forming a nonmagnetic tunnel barrier layer over said sense layer and said dielectric layer;

forming a pinned layer over said nonmagnetic tunnel barrier layer; and

patterning said pinned layer, nonmagnetic tunnel barrier layer and said dielectric layer to form a memory cell.

30. The method of claim 29 wherein said opening is a trench.

31. The method of claim 29 wherein said opening is surrounded by said dielectric layer.

32. The method of claim 29 wherein said plating is performed at about 80^0 – 90^0C.

33. The method of claim 29 wherein said step of planarizing is performed by sputtering.

34. The method of claim 29 wherein said step of planarizing is performed by chemical mechanical polishing.

35. The method of claim 29 wherein said dielectric layer is formed to a thickness of about 2-3 nm thicker than the desired thickness of said sense layer.

36. The method of claim 29 wherein said sense layer is formed of NiFe.

37. The method of claim 29 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.

38. The method of claim 29 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.

39. The method of claim 29 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

40. The method of claim 29 wherein said nonmagnetic layer is aluminum oxide.

41. A magnetic random access memory structure comprising:

a longitudinally extending planarized conductive line formed within an insulating layer;

an electroplated bottom sense layer over said conductive line;

a nonmagnetic tunnel barrier layer over said sense layer;

a pinned layer over said nonmagnetic layer; and

at least one electrical conductor in contact with said pinned layer.

42. The structure of claim 41 wherein said sense layer is formed of NiFe.

43. The structure of claim 41 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

44. The structure of claim 41 wherein said nonmagnetic layer is aluminum oxide.

45. The structure of claim 41 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.

46. The structure of claim 41 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.

47. A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a plurality of magnetic random access memory cells, each of said magnetic random access memory cells including an electroplated bottom sense layer formed over a planarized conductor, a nonmagnetic layer formed over said sense layer and a pinned layer formed over said nonmagnetic layer.

48. The system of claim 47 wherein said sense layer is formed of NiFe.

49. The system of claim 47 wherein said nonmagnetic layer is aluminum oxide.

50. The system of claim 47 wherein said sense layer is formed of plurality of layers to produce a ferromagnetic sense layer.

51. The system of claim 47 wherein said pinned layer is formed of a plurality of layers to produce a ferromagnetic pinned layer.